



***Amendments to the Claims***

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (currently amended) In scan testing of an integrated circuit with a plurality of scan paths, a method for debugging scan testing failures of the integrated circuit, comprising the steps of:
  - (a) conducting scan tests on the plurality of scan paths;
  - (b) identifying a bad scan path that is generating one or more errors within the plurality of scan paths, wherein all other scan paths within the plurality of scan paths are considered to be good scan paths;
  - (c) assessing scan test results on the bad scan path and good scan paths;
  - (d) masking the bad scan path to define defining a segment point that segments the bad scan path into two segments;
  - (e) tracing the source of errors in the bad scan path segment following the segment point when the number of errors of an output of the bad scan path following the segment point are less than a bad path error threshold and the number of errors of outputs on each of the good scan paths are less than a good path error threshold; and
  - (f) shifting the segment point based on an analysis of the errors generated by the bad scan path and the good scan paths and returning to step (b) when the number of errors of an output of the bad scan path are greater than a bad path error threshold or the number of errors on an output of any one of the good scan paths is greater than a good path error threshold.
2. (original) The method of claim 1, further comprising the step of confirming after step (a) that good scan paths are not generating errors.

3. (original) The method of claim 2, further comprising masking the bad scan path.
4. (currently amended) The method of claim 1, wherein step (a) includes running a series of scan tests ~~for on~~ the plurality of scan paths.
5. (original) The method of claim 1, wherein step (a) includes running a series of scan tests for the plurality of scan paths while varying a temperature of the integrated circuit.
6. (original) The method of claim 1, wherein step (a) includes running a series of scan tests for the plurality of scan paths while varying a test voltage.
7. (original) The method of claim 1, wherein step (a) includes running a series of scan tests for the plurality of scan paths while varying the frequency of a clock signal input.
8. (cancelled)
9. (previously presented) The method of claim 1, wherein step (d) includes determining the number of errors generated by the bad scan path following the segment point and each of the good scan paths.
10. (original) The method of claim 1, wherein in step (e) tracing the source of errors includes identifying a first error source that generated an error and determining whether the error originated within the first error source or within a coupled error source based on the relationship between the first error source and the coupled error source.
11. (original) The method of claim 9, wherein the tracing the source of errors is conducted manually.
12. (original) The method of claim 9, wherein the tracing the source of errors is conducted automatically through an automated testing unit.

13. (previously presented) The method of claim 1, wherein in step (f) when the number of errors in an output of the bad scan path following the segment point is greater than the bad scan path error threshold, shifting the segment point toward the end of the bad scan path.
14. (original) The method of claim 13, wherein the segment point is shifted such that the new segment point is midway between the end of the bad scan path and an existing segment point.
15. (previously presented) The method of claim 1, wherein in step (f) when the number of errors in an output of the bad scan path following the segment point is less than the bad scan path error threshold and the number of errors in an output of at least one good scan path is greater than the good scan path error threshold, shifting the segment point toward the beginning of the bad scan path.
16. (original) The method of claim 15, wherein the segment point is shifted such that the new segment point is midway between the beginning of the bad scan path and an existing segment point.
17. (currently amended) In scan testing of an integrated circuit with a plurality of scan paths, a method for debugging scan testing failures of the integrated circuit, comprising the steps of:
  - (a) conducting scan tests on the plurality of scan paths;
  - (b) identifying a plurality of bad scan paths that are generating one or more errors within the plurality of scan paths, wherein all other scan paths within the plurality of scan paths are considered to be good scan paths;
  - (c) assessing scan test results on the bad scan path under test and good scan paths;
  - (d) masking all bad scan paths except a bad scan path under test;

- (e) masking the bad scan path to definedefining a segment point that segments the bad scan path into two segments;
- (f) tracing the source of errors in the bad scan path segment following the segment point when the number of errors of an output of the bad scan path following the segment point are less than a bad path error threshold and the number of errors of outputs on each of the good scan paths are less than a good path error threshold;
- (g) shifting the segment point based on an analysis of the errors generated by the bad scan path and the good scan paths and returning to step (b) when the number of errors of an output of the bad scan path under test are greater than a bad path error threshold or the number of errors on an output of any one of the good scan paths are greater than a good path error threshold; and
- (h) repeating steps (b) through (g) until the source or sources of errors within all bad scan paths among said plurality of bad scan paths have been located.

18. (original) The method of claim 17, further comprising the step of confirming after step (a) that good scan paths are not generating errors.

19. (original) The method of claim 18, further comprising masking all bad scan paths.

20. (currently amended) The method of claim 17, wherein step (a) includes running a series of scan tests ~~for~~on the plurality of scan paths.

21. (cancelled)

22. (original) The method of claim 17, wherein in step (f) tracing the source of errors includes identifying a first error source that generated an error and determining whether the error originated within the first error source or within

a coupled error source based on the relationship between the first error source and the coupled error source.

23. (original) The method of claim 22, wherein tracing the source of errors is conducted manually.
24. (original) The method of claim 22, wherein tracing the source of errors is conducted automatically through an automated testing unit.
25. (previously presented) The method of claim 17, wherein in step (g) when the number of errors in an output of the bad scan path following the segment point is greater than the bad scan path error threshold, shifting the segment point toward the end of the bad scan path under test.
26. (original) The method of claim 25, wherein the segment point is shifted such that the new segment point is midway between the end of the bad scan path under test and an existing segment point.
27. (previously presented) The method of claim 17, wherein in step (g) when the number of errors in an output of the bad scan path following the segment point is less than the bad scan path error threshold and the number of errors in an output of at least one good scan path is greater than the good scan path error threshold, shifting the segment point toward the beginning of the bad scan path under test.
28. (original) The method of claim 27, wherein the segment point is shifted such that the new segment point is midway between the beginning of the bad scan path under test and an existing segment point.